George Short Schaertl

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Pronouns: they/them
Available: Summer 2018

Education

Aug. 2017– May 2019 **M.S., Electrical and Computer Engineering**(Integrated Circuits and Systems), *University of Texas at Austin*, Austin, TX, 4.00.
- Spring 2018: Microarchitecture, VLSI II, Design for Low-Power and Robustness.
- Fall 2017: Computer Architecture, VLSI I, Embedded System Design and Modeling.

June 2005– May 2009 **B.S., Electrical Engineering**, *United States Naval Academy*, Annapolis, MD, 3.83.
- Honors: Tau Beta Pi.

Experience

June 2014– Dec. 2017 **Electrical Engineer**, *Mangan Inc.*, Long Beach, CA.
- Instrumentation, control, and functional safety engineering in oil refineries.
- Reverse engineering of legacy systems; safety-critical PLC programming; on-site validation and commissioning; operating, maintenance, and test procedure development.

May 2009– May 2014 **Submarine Officer**, *United States Navy*, Kings Bay, GA / Atlantic Ocean.
- Shift supervisor for day-to-day operations, maintenance, and testing of a $2bn warship with a crew of 160. Line manager for 12 electricians and electronics technicians.

Publications

Dec. 2009 C.R. Anderson, **G. Schaertl**, and P. Balister, "A low-cost embedded SDR solution for prototyping and experimentation," in *Software Defined Radio Technical and Product Exposition (SDR'09)*, Washington, DC, Dec. 2009. [Online]. Available: http://www.kk4ead.org/beaglesdr_paper.pdf

Projects

Dec. 2017 T. Jing, R. Mital, and **G. Schaertl**, "A VLSI implementation of the FACE sorting accelerator," *VLSI I*, Univ. Texas at Austin, Dec. 2017.

Dec. 2017 B. Boesch, Y. Karundia, and **G. Schaertl**, "Comparison of high-level synthesis languages for bandwidth-intensive tasks," *Embedded System Design and Modeling*, Univ. Texas at Austin, Dec. 2017.

Dec. 2008 **G. Schaertl**, "A vector display controller and graphics processor using Altera's DE2 FPGA development board," *Microcomputer Interfacing*, U.S. Naval Academy, Dec. 2008.

Skills

Languages	C, C++, SystemC, Verilog, Python, Bash, SQLite
Tools	Virtuoso, Design Compiler, Vivado HLS, GEM5, Excel, AutoCAD (2D)
Licensing	Professional Engineer (EE, California)
Clearance	Eligible for TS/SCI (SSBI-PR, May 2014)